CHAPTER 3
Boolean Algebra and Digital Logic

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3.1 Introduction 93

• In 1854 George Boole introduced a systematic treatment of logic and developed for this purpose an algebraic system known as symbolic logic, or Boolean algebra.

• Boolean algebra is a branch of mathematics and it can be used to describe the manipulation and processing of binary information. The two-valued Boolean algebra has important application in the design of modern computing systems.

• This chapter contains a brief introduction the basics of logic design. It provides minimal coverage of Boolean algebra and this algebra’s relationship to logic gates and basic digital circuit.

3.2 Boolean Algebra 94

• Boolean algebra is algebra for the manipulation of objects that can take on only two values, typically true and false.

• It is common to interpret the digital value 0 as false and the digital value 1 as true.

3.2.1 Boolean Expressions 94

• Boolean Expression: Combining the variables and operation yields Boolean expressions.

• Boolean Function: A Boolean function typically has one or more input values and yields a result, based on these input values, in the range \{0, 1\}.

• A Boolean operator can be completely described using a table that list inputs, all possible values for these inputs, and the resulting values of the operation.

• A truth table shows the relationship, in tabular form, between the input values and the result of a specific Boolean operator or function on the input variables.

• The AND operator is also known as a Boolean product. The Boolean expression \(xy\) is equivalent to the expression \(x \times y\) and is read “\(x\) and \(y\)” The behavior of this operator is characterized by the truth table shown in Table 3.1

<table>
<thead>
<tr>
<th>Inputs (x) (y)</th>
<th>Outputs (xy)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>0</td>
</tr>
<tr>
<td>0 1</td>
<td>0</td>
</tr>
<tr>
<td>1 0</td>
<td>0</td>
</tr>
<tr>
<td>1 1</td>
<td>1</td>
</tr>
</tbody>
</table>

TABLE 3.1 The Truth Table for AND
• The OR operator is often referred to as a **Boolean sum**. The expression \( x+y \) is read “\( x \) or \( y \)”. The truth table for OR is shown in Table 3.2

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( x )</td>
<td>( y )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**TABLE 3.2 The Truth Table OR**

• Both \( \overline{x} \) and \( x' \) are read as “NOT \( x \)”. The truth table for NOT is shown in Table 3.3

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( x )</td>
<td>( \overline{x} )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**TABLE 3.3 The Truth Table for NOT**

• The rule of precedence for Boolean operators give NOT top priority, followed by AND, and then OR

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( x )</td>
<td>( y )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**TABLE 3.4 The Truth Table for \( F(x,y,z) = x + y'z \)**
3.2.2 Boolean Identities 96

- Boolean expression can be simplified, but we need new identities, or laws, that apply to Boolean algebra instead of regular algebra.

<table>
<thead>
<tr>
<th>Identity Name</th>
<th>AND Form</th>
<th>OR Form</th>
</tr>
</thead>
<tbody>
<tr>
<td>Identity Law</td>
<td>$x = x$</td>
<td>$0 + x = x$</td>
</tr>
<tr>
<td>Null (or Dominance) Law</td>
<td>$0 x = 0$</td>
<td>$1 + x = 1$</td>
</tr>
<tr>
<td>Idempotent Law</td>
<td>$x x = x$</td>
<td>$x + x = x$</td>
</tr>
<tr>
<td>Inverse Law</td>
<td>$x \bar{x} = 0$</td>
<td>$x + \bar{x} = 1$</td>
</tr>
<tr>
<td>Commutative Law</td>
<td>$x y = y x$</td>
<td>$x + y = y + x$</td>
</tr>
<tr>
<td>Associative Law</td>
<td>$(x y) z = x (y z)$</td>
<td>$(x + y) + z = x + (y + z)$</td>
</tr>
<tr>
<td>Distributive Law</td>
<td>$x + y z = (x + y) (x + z)$</td>
<td>$x (y + z) = xy + x z$</td>
</tr>
<tr>
<td>Absorption Law</td>
<td>$x (x + y) = x$</td>
<td>$x + x y = x$</td>
</tr>
<tr>
<td>DeMorgan’s Law</td>
<td>$(x \bar{y}) = \bar{x} + \bar{y}$</td>
<td>$(x + \bar{y}) = \bar{x} \bar{y}$</td>
</tr>
<tr>
<td>Double Complement Law</td>
<td>$\bar{\bar{x}} = x$</td>
<td></td>
</tr>
</tbody>
</table>

### TABLE 3.5 Basic Identities of Boolean Algebra

- **DeMorgan’s** law provides an easy way of finding the complement of a Boolean function.

\[
(xy) = \bar{x} + \bar{y} \quad \text{and} \quad (x + y) = \bar{x} \bar{y}
\]

<table>
<thead>
<tr>
<th>$x$</th>
<th>$y$</th>
<th>$(xy)$</th>
<th>$(\bar{x} \bar{y})$</th>
<th>$\bar{x}$</th>
<th>$\bar{y}$</th>
<th>$\bar{x} + \bar{y}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
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<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

### TABLE 3.6 Truth Tables for the AND Form of DeMorgan’s Law

3.2.3 Simplification of Boolean Expressions 98

- The algebraic identities we studied in algebra class allow us to reduce algebraic expression to their simplest form.
- EXAMPLE 3.2
- EXAMPLE 3.3
• How did we know to insert additional terms to simplify the function? Unfortunately, there no defined set of rules for using these identities to minimize a Boolean expression: it is simply something that comes with experience.
• To prove the equality of two Boolean expressions, you can also create the truth tables for each and compare. If the truth tables are identical, the expressions are equal.

<table>
<thead>
<tr>
<th>Proof</th>
<th>Identity Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>((x+y)(\overline{x}+y)) = xx+x+y\overline{x}+yy</td>
<td>Distributive Law</td>
</tr>
<tr>
<td>= 0+xy+y\overline{x}+yy</td>
<td>Inverse Law</td>
</tr>
<tr>
<td>= 0+xy+y\overline{x}+y</td>
<td>Idempotent Law</td>
</tr>
<tr>
<td>= xy+y\overline{x}+y</td>
<td>Identity Law</td>
</tr>
<tr>
<td>= y(x+\overline{x})+y</td>
<td>Distributive Law (and Commutative Law)</td>
</tr>
<tr>
<td>= y(1)+y</td>
<td>Inverse Law</td>
</tr>
<tr>
<td>= y+y</td>
<td>Identity Law</td>
</tr>
<tr>
<td>= y</td>
<td>Idempotent Law</td>
</tr>
</tbody>
</table>

TABLE 3.7 Example using Identities

3.2.4 Complements 99

<table>
<thead>
<tr>
<th>Proof</th>
<th>Identity Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>((x+y)(\overline{x}+y)) = xx+x+y\overline{x}+yy</td>
<td>Distributive Law</td>
</tr>
<tr>
<td>= 0+xy+y\overline{x}+yy</td>
<td>Inverse Law</td>
</tr>
<tr>
<td>= 0+xy+y\overline{x}+y</td>
<td>Idempotent Law</td>
</tr>
<tr>
<td>= xy+y\overline{x}+y</td>
<td>Identity Law</td>
</tr>
<tr>
<td>= y(x+\overline{x})+y</td>
<td>Distributive Law (and Commutative Law)</td>
</tr>
<tr>
<td>= y(1)+y</td>
<td>Inverse Law</td>
</tr>
<tr>
<td>= y+y</td>
<td>Identity Law</td>
</tr>
<tr>
<td>= y</td>
<td>Idempotent Law</td>
</tr>
</tbody>
</table>

TABLE 3.8 Truth Table Representation for a Function and Its Complement

3.2.5 Representing Boolean Functions 100
• In fact, there are an infinite number of Boolean expressions that are logically equivalent to one another.
• Two expressions that can be represented by the same truth table are considered logically equivalent.
• EXAMPLE 3.4
• The two most common standardized forms are the **sum-of-products** form and the **product-of-sums** form.

• In the **sum-of-products** form, ANDed variables are ORed together. For example,

$$\quad F(x, y, z) = xy + xz + yz$$

• In the **product-of-sums** form, ORed variables are ANDed together. For example,

$$\quad F(x, y, z) = (x+y) (x+z) (y+z)$$

• The sum-of-products form is usually easier to work with and to simplify, so we use this form exclusively in the sections that follow.

• It is easy to convert a function to **sum-of-products** form using its truth table.

• We are interested in the values of the variables that make the function true (=1). Using the truth table, we list the values of the variables that result in a true function value.

• Each group of variables is then ORed together.

• **EXAMPLE 3.5**

<table>
<thead>
<tr>
<th>$x$</th>
<th>$y$</th>
<th>$z$</th>
<th>$F$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>1</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**TABLE 3.9 Truth Table Representation for the Majority Function**

sum-of-products: $F(x, y, z) = x'yz + xy'z + xyz' + xyz$

### 3.3 Logic Gates 102

• We see that Boolean functions are implemented in digital computer circuits called **gates**.

• A gate is an electronic device that produces a **result** based on two or more input values.

• In reality, gates consist of one to six **transistors**, but digital designers think of them as a single unit.

• Integrated circuits contain collections of gates suited to a particular purpose.
3.3.1 Symbols for Logic Gates 102

- The three simplest gates are the AND, OR, and NOT gates.

![FIGURE 3.1 The Three Basic Gates](image)

- Another very useful gate is the exclusive OR (XOR) gate.
- The output of the XOR operation is true only when the values of the inputs differ.

![FIGURE 3.2 The exclusive OR (XOR) Gate](image)

3.3.2 Universal Gates 103

- Two other common gates are NAND and NOR, which produce complementary output to AND and OR.

![FIGURE 3.3 and 3.4 The Truth Table and Logic Symbols for NAND and NOR Gates](image)
• NAND and NOR are known as **universal gates** because they are **inexpensive** to manufacture and any Boolean function can be constructed using only NAND or only NOR gates.

![Three Circuits Constructed Using Only NAND Gates](image)

**FIGURE 3.5 Three Circuits Constructed Using Only NAND Gates**

### 3.3.3 Multiple Input Gates 104
• Gates can have multiple inputs and more than one output.

![Multiple Gates](image)

**FIGURE 3.6, 3.7, and 3.8**

### 3.4 Digital Components 105
• Every computer is built using collections of **gates** that are all connected by way of wires acting as signal gateway.

### 3.4.1 Digital Circuits and Their Relationship to Boolean Algebra 105
• More complex Boolean expressions can be represented as combinations of AND, OR, and NOT gates, resulting in a logic diagram that describes the entire expression.

![Logic Diagram](image)

**FIGURE 3.9 A Logic Diagram for F(x, y, z) = x + y’z**
3.4.2 Integrated Circuits 106

- Gates are not sold individually; they are sold in units called integrated circuits (ICs).
- A chip (a small silicon semiconductor crystal) is a small electronic device consisting of the necessary electronic components (transistors, resistors, and capacitors) to implement various gates.
- The first IC were called SSI chips and contained up to 100 electronic components per chip.
- We now have ULSI (ultra large-scale integration) with more than 1 million electronic components per chip.

![Image of a simple SSI Integrated Circuit]

3.5 Combinational Circuits 106

- Digital logic chips are combined to give us useful circuits. These logic circuits can be categorized as either combinational logic (Section 3.5) or sequential logic (Sec. 3.6).

3.5.1 Basic Concepts 107

- The key concept in recognizing a combinational circuit is that an output is always based on the given inputs.
- The output of a combinational circuit is a function of its inputs, and the output is uniquely determined by the values of the inputs at any given moment.
- A given combinational circuit may have several outputs. If so, each output represents a different Boolean function.

3.5.2 Examples of Typical Combinational Circuits 107

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>Y</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

![Image of a half-adder]

TABLE 3.10 and FIGURE 3.11 The Truth Table and The Logic Diagram for a Half-Adder
• Note that this full-adder is composed of two half-adder

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>Y</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

FIGURE 3.12 The Truth Table and The Logic Diagram for a Full-Adder
Sum = X xor Y xor C_in; Cout = XY + (X xor Y) C_in

• Decoder: Decoding binary information from a set of n inputs to a maximum of $2^n$ outputs.
• A decoder uses the inputs and their respective values to select one specific output line.
• One unique output line is set to 1, while the other output lines are set to 0.
• A decoder that has 3 inputs and 8 outputs is called a 3-to-8 decoder.

FIGURE 3.13 The Logic Diagram for a Ripple-Carry Adder

• EXAMPLE 3.6 A 3-to-8 decoder circuit
  o Imagine memory consisting of 8 chips, each containing 8K bytes.
  o We have a total of 8K * 8, or 64K (65,536) address available.
  o We need 16 bits to represent each address.
  o The leftmost 3 bits determine on which chip the address is actually located. All addresses on chip 0 have the format: 000X XXXX XXXX XXXX: Because chip 0 contains the address 0-8191. Similarly, all addresses on the chip 1 have the format: 001X XXXX XXXX XXXX.
The 3 high-order bits are actually used as the inputs to a decoder so the computer can determine which chip to activate for reading or writing.

The output of the decoder is used to activate one, and only one, chip as the addresses are decoded.

- The **Multiplexer** circuits binary information from one of many input lines and directs it to a single output line.
- Only one input (the one selected) is routed through the circuit to output line. All other inputs are “cut off.”
- Can you think of some situations that require multiplexers? **Time-sharing** computers multiplex the input from user terminals. Modem pools multiplex the modem lines entering the computer.

![FIGURE 3.15 a) A Look Inside a Multiplexer; b) A Multiplexer Symbol](image)

- A **parity generator** is a circuit that creates the necessary parity bit to add to a word.
- A **parity checker** checks to make sure proper parity (odd or even) is present in the word.
- Typically parity generators and parity checkers are constructed using **XOR** functions. Assuming we are using **odd** parity, the truth table for a parity generator for a 3-bit word is given in Table 3.11.
- The parity checker outputs a 1 if an **error** is detected and 0 otherwise.

<table>
<thead>
<tr>
<th>x</th>
<th>y</th>
<th>z</th>
<th>Parity Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 3.11 Parity Generator

<table>
<thead>
<tr>
<th>x</th>
<th>y</th>
<th>z</th>
<th>Error detected?</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 3.12 Parity Checker
• Figure 3.16 illustrates a very simple ALU with four basic operations – **AND**, **OR**, **NOT**, and addition – carried out on two machine words of 2 bits each.
• The control lines, \( f_0 \) and \( f_1 \), determine which operation is to be performed by the CPU.
• The signal **00** is used for addition \( (A + B) \); **01** for \( \text{NOT } A \); **10** for \( A \text{ OR } B \), and **11** for \( A \text{ AND } B \).
• The input lines \( A_0 \) and \( A_1 \) indicate 2 bits of one word, while \( B_0 \) and \( B_1 \) indicate the second word, \( C_0 \) and \( C_1 \) represent the output lines.

![FIGURE 3.16 A Simple Two-Bit ALU](image-url)
3.6 Sequential Circuits 113

- The major **weakness** of **combinational circuits** is that there is no concept of storage – they are **memoryless**. If we change an input value, this has a direct and **immediate** impact on the value of the output.

3.6.1 Basic Concepts 114

- A sequential circuit defines its output as a function of both its current inputs and its previous inputs. Therefore, the output depends on **past** inputs.
- We typically refer to this storage element as a **flip-flop**.
- Combinational circuits are generalizations of **gates**; sequential circuits are generalizations of **flip-flops**.

3.6.2 Clocks 114

- A sequential circuit uses **past inputs** to determine **present outputs** indicates we must have event ordering.
- A clock is a circuit that emits a series of pulses with a precise pulse width and a precise **interval** between consecutive pulses.
- This interval is called the **clock cycle time**. Clock speed is generally measured in megahertz (MHz), or millions of pulse per second.
- A clock is used by a **sequential circuit** to decide **when** to update the state of the circuit.
- Most sequential circuits are **edge-triggered** (as opposed to being level-triggered). It means they are allowed to change their state on either the **rising** or **falling** edge of the clock signal.

![FIGURE 3.17 A clock Signal Indicating Discrete Instances of Time](image)

3.6.3 Flip-Flops 115

- Many people use the terms **latch** and flip-flop interchangeably. Technically, a latch is level triggered, whereas a flip-flop is edge triggered.
- In order to “remember” a past state, sequential circuits rely on a concept called **feedback**. This simply means the output of a circuit is fed back as an input to the same circuit.

![FIGURE 3.18 Example of Simple Feedback](image)
• A more useful feedback circuit is composed of two NOR gates resulting in the most basic memory unit call an **SR flip-flop**. SR stands for “set/reset.”

![SR Flip-Flop Logic Diagram](image)

**FIGURE 3.19 A SR Flip-Flop Logic Diagram**

• Q(t) means the value of the output at time t. Q(t+1) is the value of Q after the next clock pulse.
• When both S and R are 1, the SR flip-flop is **unstable**.

![Actual SR Flip-Flop and Characteristic Table](image)

**FIGURE 3.20 a) The Actual SR Flip-Flop; b) The Characteristic Table for the SR Flip-Flop**

• The SR flip-flop actually has three inputs: S, R, and its current output, Q.

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>S  R  Q(t)</td>
<td>Q(t+1)</td>
</tr>
<tr>
<td>0  0  0</td>
<td>0</td>
</tr>
<tr>
<td>0  0  1</td>
<td>1</td>
</tr>
<tr>
<td>0  1  0</td>
<td>0</td>
</tr>
<tr>
<td>0  1  1</td>
<td>0</td>
</tr>
<tr>
<td>1  0  0</td>
<td>1</td>
</tr>
<tr>
<td>1  0  1</td>
<td>1</td>
</tr>
<tr>
<td>1  1  0</td>
<td>undefined</td>
</tr>
<tr>
<td>1  1  1</td>
<td>undefined</td>
</tr>
</tbody>
</table>

**TABLE 3.13 Truth Table for SR Flip-Flop**
• A **JK flip-flop** simply modify the SR flip-flop to ensure that the **illegal state** (both S and R are 1) never arises.
• The inputs to an SR flip-flop will **never** both be 1
• We will never have an **unstable** circuit.

![JK and SR Flip-Flop Diagrams](image)

**FIGURE 3.21** a) A JK Flip-Flop; b) The JK Characteristic Table c) A JK Flip-Flop as a Modified SR Flip-Flop

• A **D flip-flop** is a **true** representation of physical computer memory.
• An output value of 1 means the circuit is currently “**storing**” a value of 1.

![D Flip-Flop Diagrams](image)

**FIGURE 3.22** a) A D Flip-Flop; b) The D Characteristic Table c) A D Flip-Flop as a Modified SR Flip-Flop
3.6.4 Examples of Sequential Circuits 117

- The registers must all accept their new input values and change their storage elements at the same time.

![A 4-Bit Register; A Block Diagram for a 4-Bit Register](image)

- If we begin counting in binary: 0000, 0001, 0010, 0011, ..., 1111, we can see that as the numbers increase, the low-order bit is complemented each time.
- When J and K are both equal to 1, the flip-flop complements the present state.
- The circuit counts only when the clock pulses and this count enable line is set to 1.

![A 4-Bit Synchronous Counter Using JK Flip-Flops](image)
• The memory depicted holds **four 3-bit words (4 X 3 memory)**.
• A read or write operation always reads or writes a **complete** word.
• The input In0, In1, In2 are lines used to **store, or write**, a 3-bit word to memory.
• The lines S0 and S1 are the **address** lines used to select which word in memory is being referenced (Notice that S0 and S1 are the input lines to a **2-to-4 decoder** that is responsible for selecting the correct memory word.)
• The output lines (Out0, Out1, and Out2) are used when **reading** words from memory.
• The write enable control line indicates whether we are **reading or writing**.
• In practice, the input lines and output lines are the **same lines**.
• To summarize our discussion of this memory circuit, here are the steps necessary to write a word to memory:
  1) An address is asserted on S0 and S1.
  2) WE (write enable) is set to high
  3) The decoder using S0 and S1 enables only one AND gate, selecting a given word in memory
  4) The line selected in Step 3 combined with the clock and WE select only one word
  5) The write gate enabled in Step 4 drives the clock for the selected word.
  6) When clock pulses, the word on the input lines is loaded into the D flip-flops.

**FIGURE 3.25 A 4 X 3 Memory**
3.7 Designing Circuits 120

- Digital logic design requires someone not only familiar with digital logic, but also well versed in digital analysis (analyzing the relationship between inputs and outputs), digital synthesis (starting with a truth table and determining the logic diagram to implement the given logic function), and the use of CAD (computer-aided design) software.

- A circuit designer faces many problems, including:
  - finding efficient Boolean functions,
  - using the smallest number of gates,
  - using an inexpensive combination of gates,
  - organizing the gates of a circuit board to use the smallest surface area and minimal power requirements, and
  - attempting to do all of this using a standard set of modules for implementation.

- Digital systems designers must also be mindful of the physical behaviors of circuits to include minute propagation delays that occur between the time when a circuit’s inputs are energized and when the output is accurate and stable.

- A circuit designer can implement any given algorithm in hardware (recall the Principle of Equivalence of Hardware and Software from chapter 1).

- When we need to implement a simple, specialized algorithm and its execution speed must be as fast as possible; a hardware solution is often preferred.

- This is the idea behind embedded systems, which are small special-purpose computers that we find in many everyday things. Your microwave oven and your car most likely contain embedded systems.

- Programming these embedded systems required design software that can read input variables and send output signals to perform such tasks as turning a light on or off, emitting a beep, sounding an alarm, or opening a door.

- Embedded systems require special programming that demands an understanding of the operation of digital circuits, the basics of which you have learned in this chapter.

Chapter Summary 121

- Computers are implementations of Boolean logic.
- Any Boolean functions can be represented as truth tables.
- Truth tables provide us with a means to express the characteristics of Boolean functions as well as logic circuits.
- There is a one-to-one correspondence between a Boolean function and its digital representation.
- From a chip designer’s point of view, the two most important factors are speed and cost: minimizing the circuits helps to both lower the cost and increase performance.
- Computer circuits consist of combinational logic circuits and sequential logic circuits.
- Combinational circuits produce outputs (almost) immediately when their inputs change.
- Sequential circuits require clocks to control their changes of state.
• Combinational logic devices, such as adders, decoders, and multiplexers, produce outputs that are based strictly on the current inputs.
• The AND, OR, and NOT gates are the building blocks for combinational logic circuits, although universal gates, such as NAND and NOR, could also be used.
• Sequential logic devices, such as registers, counters, and memory, produce outputs based on the combination of current inputs and the current state of the circuits. These circuits are built using SR, D, and JK flip-flops.
Focus on Karnaugh Maps 130

3A.1 Introduction 130

- **Minimizing** circuits helps reduce the number of components in the actual physical implementation.
- Reducing Boolean expressions can be done suing Boolean identities; however, using identities can be very difficult because **no rules** are given on how or when to use the identities.
- In this appendix, we introduce a systematic approach for reducing Boolean expression.

3A.2 Description of Kmaps and Terminology 131

- Karnaugh maps, or Kmaps, are **graphical** way to represent Boolean functions.
- For example, if there are two input values, x and y, there are four minterms.

- EXAMPLE 3A.1 \( F(x, y) = xy \)

- EXAMPLE 3A.2 \( F(x, y) = x + y \)

\[
\begin{align*}
F(x, y) &= xy \\
F(x, y) &= x + y
\end{align*}
\]
3A.3 Kmap Simplification for Two Variables 133

- The rules of Kmap simplification are:
  1) **Groupings** can contain only 1s; no 0s.
  2) Only 1s in **adjacent** cells can be grouped; diagonal grouping is not allowed.
  3) The number of 1s in a group must be a **power of 2**.
  4) The groups must be made as **large** as possible while still following all rules.
  5) All 1s must belong a group, even if it is a group of one.
  6) **Overlapping** groups are allowed.
  7) **Wrap** around is allowed.
  8) Use the **fewest** number of groups possible.

![Figure 3A.3 Kmap for F(x, y) = x + y](image)

3A.4 Kmap Simplification for Three Variables 134

- **EXAMPLE 3A.3**

\[ F(x, y, z) = \overline{xyz} + \overline{xyz} + \overline{xyz} + \overline{xyz} \]

![Figure 3A.8 Minterms and Kmap Format for Three Variables](image)

- It reduces to \( F(x, y, z) = z \)
EXAMPLE 3A.4

\[ F(x, y, z) = x'y'z' + x'y'z + x'yz + x'y'z + x'yz + x'y + xyz \]

\[
\begin{array}{c|cccc}
  & YZ & 00 & 01 & 11 & 10  \\
  X & \hline 
  0 & 1 & 1 & 1 & 1 \\
  1 & 1 & 0 & 0 & 1 \\
\end{array}
\]

It reduces to \( F(x, y, z) = x' + z' \)

3A.5 Kmap Simplification for Four Variables 137

![Kmap Format](image)

FIGURE 3A.8 Minterms and Kmap Format for Four Variables

EXAMPLE 3A.6

\[ F(w, x, y, z) = \bar{w}xyz + \bar{w}x'yz + w'y'z' + \bar{w}x'z + w'yz + w'xz + \bar{w}xz + \bar{w}y'z \]

\[
\begin{array}{c|cccc}
  & WZ & 00 & 01 & 11 & 10  \\
  W & \hline 
  00 & 1 & 1 & 1 & 1 \\
  01 & 1 & 1 & 1 & 1 \\
  11 & 1 & 1 & 1 & 1 \\
  10 & 1 & 1 & 1 & 1 \\
\end{array}
\]

\[ F(w, x, y, z) = \bar{x}y + \bar{x}z + \bar{w}y'z \]

EXAMPLE 3A.7

The last terms are different. \( F_1 \) and \( F_2 \), however, are equivalent.

If we follow the rules, Kmap minimization results in a minimized function (and thus a minimal circuit), but these minimized functions need not be unique in representation.

\[
\begin{array}{c|cccc}
  & WZ & 00 & 01 & 11 & 10  \\
  W & \hline 
  00 & 1 & 1 & 1 & 1 \\
  01 & 1 & 1 & 1 & 1 \\
  11 & 1 & 1 & 1 & 1 \\
  10 & 1 & 1 & 1 & 1 \\
\end{array}
\]

\[ F(w, x, y, z) = F_1 = y'z' + w'yz + w'xz \quad F(w, x, y, z) = F_2 = y'z' + w'yz + w'xz \]
3A.6 Don’t Care Conditions 140

- There are certain situations where a function may not be completely specified, meaning there may be some inputs that are **undefined** for the function.
- **Real circuits don’t** always need to have an **output** defined for every possible input.
- If a circuit is designed so that a particular set of inputs can **never happen**, we call this set of inputs a **don’t care** condition.
- They are very **helpful** to us in Kmap circuit simplification. Because they are input values that should not matter (and should never occur), we can let them have values of **either 0 or 1**, depending on which helps us the most.
- Don’t care values are typically indicated with an “**X**” in the appropriate cell.
- **EXAMPLE 3A.10**

\[
F (W, X, Y, Z) = \overline{W}X + YZ
\]

\[
F (W, X, Y, Z) = \overline{W} + YZ
\]

3A.7 Summary 141

- Using Boolean identities for reduction is awkward and can be very difficult.
- Kmaps provide a precise of steps to follow to find the minimal representation of a function, and thus the minimal circuit that function represents.
- The rules of Kmap simplification are:
  1) Groupings can contain only 1s; no 0s
  2) Only 1s in **adjacent** cells can be grouped; diagonal grouping is not allowed.
  3) The number of 1s in a group must be a **power of 2**.
  4) The groups must be made as **large** as possible while still following all rules.
  5) All 1s must belong a group, even if it is a group of one.
  6) **Overlapping** groups are allowed.
  7) **Wrap** around is allowed.
  8) Use the **fewest** number of groups possible.