

Reverse Engineering of Real PCB Level Design Using VERILOG HDL

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Abstract

The repair or replacement of components nearing obsolescence and the lack of accuracy in technical information is a very common problem. Updating these systems is possible now with sophisticated CAE tools and the Hardware Description Languages. Here we consider the conversion process of a real board design from TTL implementation to newer technology. This process is performed through an Automatic Verilog HDL Model Generator, which includes an image analysis system, for component identification(integrated circuits) and their connections. On the basis of the information obtained, the system is able to generate a circuit graph that corresponds to a primitive schematic circuit of the board. The circuit graph is translated to VERILOG HDL. The tests were performed in Verilog XL simulator. Therefore the system is capable to reverse engineer a board level design performed with a nondestructive procedure.

1. Introduction

The electronics systems technology is improving day by day. This natural development generates a big amount of systems that will become obsolete quickly. Those legacy systems are old but still valuable. the main problems are:

1.- The piece parts, modules, IC's, etc. Are out of stock or have been superseded. Therefore it is very hard to acquire them.

2- Incomplete technical information or the technical information is not available.

3.- In particular cases the system technical information is not always updated after some modifications have been performed. The real system does not conform to the posted technical information.

The legacy systems and the systems that are nearing obsolescence should migrate toward the new technologies for increase their life cycle. In areas such as medical, industrial, research and military there exists a special interest in updating their systems with present technology.

The goal of this paper is to use image processing, to obtain a description system functionality and convert this description to Verilog XL as part of a migration process toward new technology.

The conversion of existing hardware to new technologies has been targeted by the Motorola Computer Group [Crate 96]. They have performed the process based on the schematic circuit and using CAE tools to generate the equivalent system with new technology. Alta group of Cadence has presented a methodology to move to system-on-chip design from the system level[Usse 97]. These are good examples of current approaches to system conversion.

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Table No. 1		
Features and Requirements	<ul style="list-style-type: none"> * No technical information is available * Incomplete information * Modified Systems * Repaired Systems * No Schematic available * Conversion from TTL 	<ul style="list-style-type: none"> * Complete Technical Information * Require Schematic * Netlist or ABEL code * Conversion from TTL or PLD
Migration Methodology	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Legacy Systems</p> <p>Standard Systems Technologies</p> <p>Reverse Engineering Re-Engineering</p> <p>↓</p> <p>New Technology</p> </div> <div style="text-align: center;"> <p>Legacy Systems</p> <p>Standard Systems Technologies</p> <p>Conversion Model</p> <p>↓</p> <p>New Technology</p> </div> </div>	

Table No. 1 shows the two general cases of migration methodology. The standard conversion method is based on the references shown earlier. Table 1 also shows the differences of the two approaches. The main difference between the migration methodologies is the inclusion of the new Reverse Engineering (RE) process, which is performed with a real board design avoiding the inaccuracy in the new model. The traditional RE method offers a complete technical data package based on existing information [DoD 87]. This process has well defined steps, but requires a lot of time in performing each one, and requires qualified personnel [Trab 96]. The new RE idea [Bour-91, Mog-93, Gat-97, Gall 98, Bour-2yk], included in this work, reduces time and increases the accuracy through an automatic and non-destructive method.

2. Conversion Methodology

The conversion methodology is based on an Automatic Verilog HDL Model Generator (AVMG), shown in Fig. 1. The AVMG includes RE tasks to extract information from a real PCB with a better and practical methodology and minimum operator intervention.

The AVMG system generates the structural description of the legacy system in Verilog HDL code. This structural

description requires tests and adjustments. These tests will verify that the original features have not been modified and the new system actually performs each of their original tasks. To support this tendency for implementing “system on chip”, the new technology design is converted to a physical model. The physical implementation can be performed in FPGA technology. Companies like Xilinx and Altera offer powerful tools that easily map Verilog to FPGA. When the legacy system is large, some parts can not be mapped in a FPGA, therefore they should be implemented in standard updated IC’s.

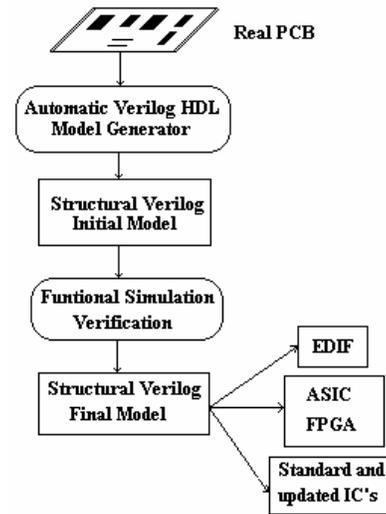


Figure 1. Conversion methodology

An essential part of the legacy systems conversion is the generation of technical information. Converting the new design in EDIF format we can generate a complete set of technical information (schematic, netlist, etc).

We are assuming only single or double sided boards but no wafer boards. To handle wafer type of boards, we would need to additionally obtain X-ray images and process them in coordination with optical images. To figure out spatial relationships of wire paths we would have

to have images from at least two different positions (so as to get spatial perspective) and additionally solve image registration problems in order to automate the process. In this work we have not extended to such possibilities which could be the focus for further work.

3. AVMG System Architecture

The general AVMG system is shown in figure No. 2.

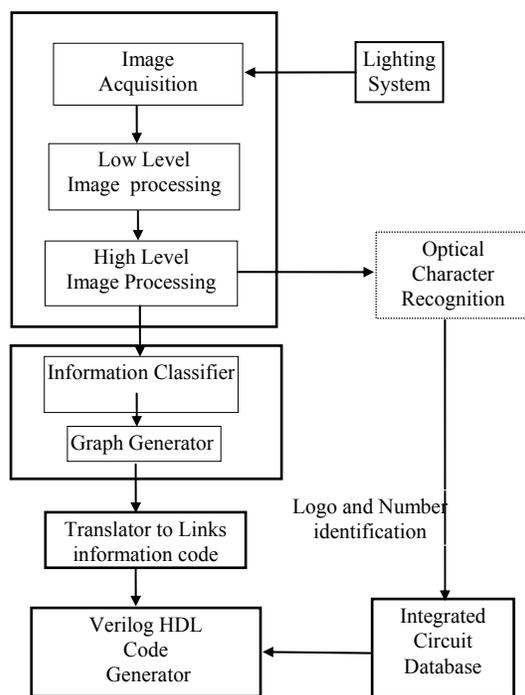


Figure 2. Overall AVMG system configuration

The system includes basically four systems:

- **Image analysis**

In this subsystem the PCB (Printed Circuit Board) image is digitized through a basic computer vision equipment. The enhancement and segmentation are

carried out. Then the shapes and their connections are recognized.

- **Graph generator**

This subsystem classifies the information and generates a primitive graph that represents the circuit elements and their connections.

- **Links Generator**

The subsystem interprets and converts the primitive graph in a link list.

- **HDL code generator**

Generate code for Verilog XL, converting from a real PCB to HDL model.

After the code is generated, it is necessary to perform some tests in order to do adjustments. The purpose of these adjustments is to integrate the circuit information and verify the system functionality. Likewise, we can simulate and generate its equivalent circuit, substituting the original and offering an equivalent with additional features in a new technology format. The simulations are carried out in VERILOG XL. Many leading-edge electronic designers use Verilog because it has great capabilities for gate level simulation and modeling at higher levels of abstraction [Cade 94]. It is already used by a lot of IC designers and supported by most EDA, FPGA, and ASIC vendors. It has over 20000 users and more than 90 products from 50 EDA vendors. [David 93]. Considering these facts, our work has been performed on Verilog. The figure 3 shows the outputs files in each model generator stage.

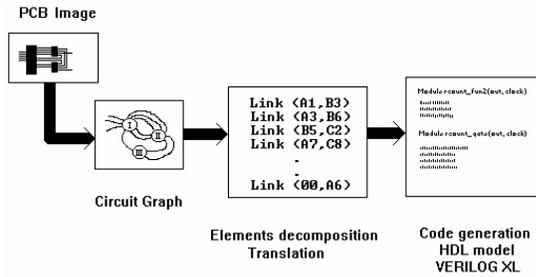


Figure 3. Output representation of each AVMG steps

3.1 Image Analysis System

The image is processed with traditional image processing techniques. The image acquisition is carried out with a basic vision system that includes a video source and frame grabber card. The images are stored in files with GIF and PCX format. The resolution is 640 X 480 pixels. The Fig 4 shows an image sample.

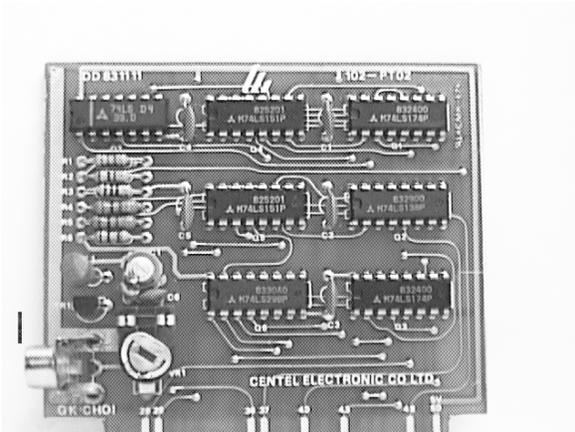


Figure 4. Real PCB image

The preprocessing for image improvement, the edge detection, thresholding, image segmentation and recognition are performed with traditional image processing techniques. The image processing is implemented on the C language, Cantata and Khoros software. The Structural methods (Matching Shape number) [Gonz 92], are used in order to identify and recognize IC's shape.

Part of this process is stated in figures 4a, 4b and 5a

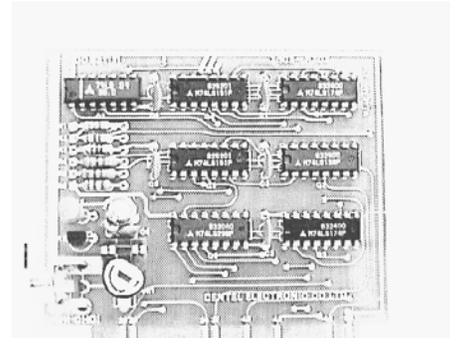


Figure 4a. Enhancing IC's for identification

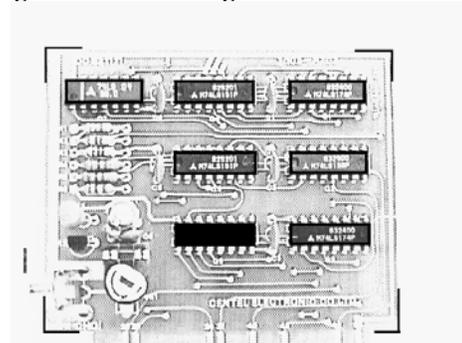


Fig 4b. IC's identification and board location

The connectivity interpretation is performed with a modified non-referential method used on PCB inspection Fig 5.b.

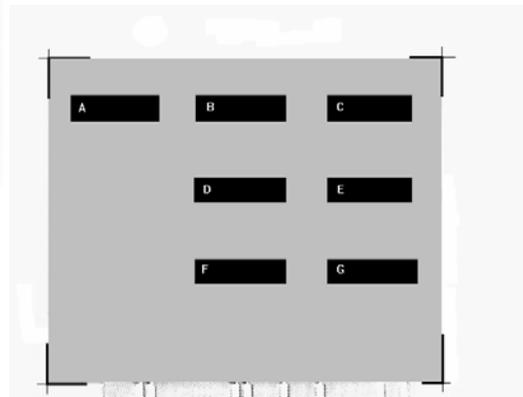


Figure 5a. Image with IC's identified

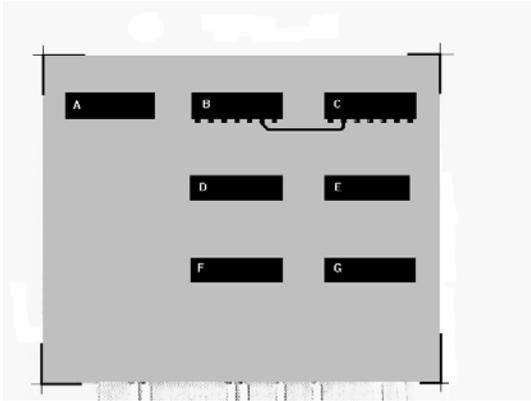


Fig 5b. Link identified between B and C IC's

The number, type, family of each IC is provided by an OCR system. In extreme identification problems the OCR system is assisted by external identification resources. The identification of each IC with manufacturer codes permits to have a preliminary idea of the general system functions.

3.2 Circuit graph

The circuit graph represents a graphical synthesis of the information extracted from the PCB in the previous steps. It includes the basic information of the circuit, which is a representation of a real image. The internal format upon which the graph is elaborated can be transformed in GERBER format. Fig 6 shows an example of the graph obtained after the image processing.

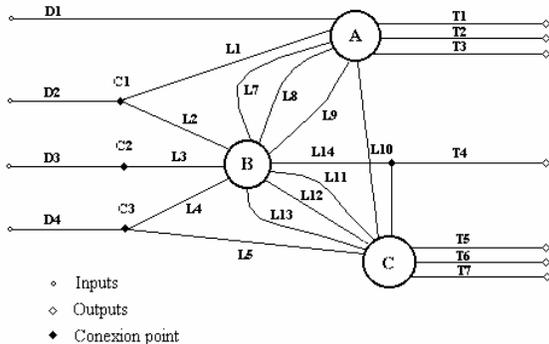


Figure 6. Circuit Primitive Graph

3.3 Graph translator to links (report generation)

With the primitive graph completely defined, a system report is generated. It is a list that describes the overall connectivity of the system. This is shown in figure 7.

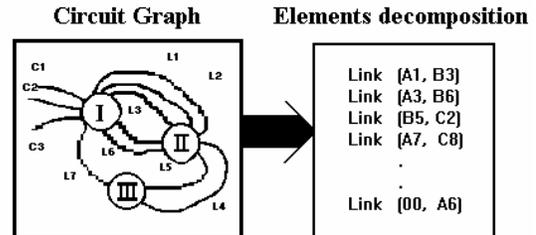


Figure 7. Primitive Graph to Links

This report includes the links between each circuit element, specifying the starting pin and the ending pin. For example, in figure 7 there is a link between pin number 1 of the integrated circuit A and pin number 3 of the integrated circuit B.

Link (A1, B3) means A1 → B3

Pin No. 1 of device A, goes to Pin No 3 of B

The next link is between pin number 3 of the IC "A" and pin 6 of the element "B" and so on.

3.4 Translation to Verilog HDL model

The final part of AVMG is the translation of the links report to Verilog HDL code. The representation of legacy systems in the new technology basically is done in this part.

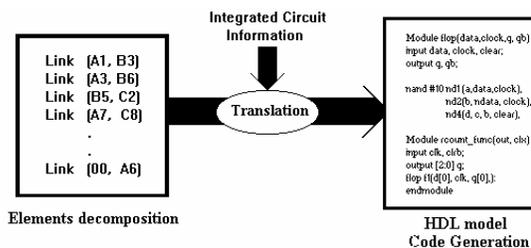


Figure 8. Code Generation

The information related with the IC's should have a standard format for its interpretation. It

consists of ordering links information, TTL libraries as well as the IC's data information. The information that corresponds to each one of the IC's is provided by an external source.

The translation is divided in two parts: *Structural representation* which prepares the information required by the translator, and the *Code generation* which is in itself the result of the conversion process. The output code, can be used as an input file and will be understood by the VERILOG XL interpreter. Having the final output, Verilog can perform any simulation and test. The AVMG is able to map from a real system to an HDL system. Nevertheless, special considerations should be made about delay time. In the code generation process the internal delay of the IC's is assigned. The delay is assigned based on the standard of the logic family used. In the last part an internal time adjustment should be performed. This is possible thanks to global variable controls of time simulation included in Verilog.

4. Model example

A simple two-four decoder unit built with TTL circuits is used to demonstrate this methodology. The image processing part has been carried out with the procedure stated earlier. Image improvement, image description, and image identification are the steps which give the complete IC's information, their location and links. After the image processing part, two IC's and their connections have been identified. The system decoder has a couple of integrated circuits (74LS00 and 74LS04) which have been identified by an OCR system. The circuit's equivalent graph is shown in Fig 9.

A complete links set is extracted from the circuit graph. It shows information of the internal connection between the chips as well as the I/O connections. These connections come from external circuits. They could be input, data activation or output data.

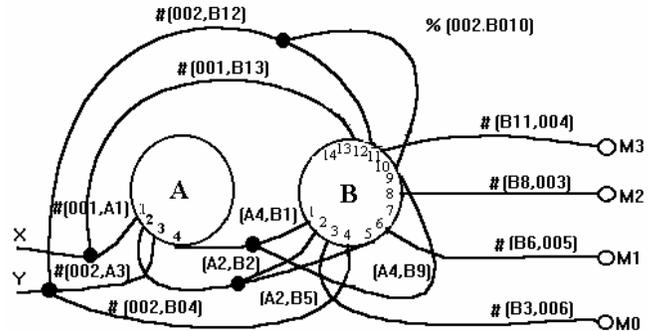


Figure 9. Decoder 2/4 decoder

The system graph is converted in a set of 14 links that represent the particular connections between the IC's for this system.

```

link!(0002,B012)
link!(0001,B013)
link!(0002,B010)
link%(B011,0004)
link%(B008,0003)
link%(B006,0005)
link%(B003,0006)
link!(0001,A001)
link!(0002,A003)
link*(A004,B001)
link*(A002,B002)
link*(A002,B005)
link!(0002,B004)
link*(A004,B009)

```

The symbols (*, !, %) included in the link representation, indicate where the links come from. Table 2 shows the link types and their symbols.

Table No.2	
Link between	Symbol
IC - IC	*
Input - IC	!
IC - Output	#

description and connectivity identification. We will improve the system capabilities for two faced and wafers PCB's.

6. Summary and Conclusion

In this paper, we have shown that it is possible to reverse engineer old systems, and convert them from legacy systems to new technology.

The systems with SSI, MSI, LSI and VLSI components can be implemented completely or in parts on ASIC and FPGA, due to the new design are independent of any implementation media.

The migration process presented in this paper includes basically the following steps:

- To get legacy system information through a real image(AVMG).
- To convert legacy system in a new verilog structural representation(AVMG).
- To test and verification of the new design functionality .
- Implementation in standard and updated IC's or in ASIC(FPGA).

Timing is an inherent conversion problem, which increase with the legacy system complexity.

The conversion methodology stated can be used for:

- Systems characterization.
- Equivalent models' comparison.
- Rapid prototype
- Obtaining of equivalent circuits.
- Design architecture Identification.
- Replacement of aged (obsolete) digital IC's
- New alternatives for hard-to-get IC's

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